

FIG. 1

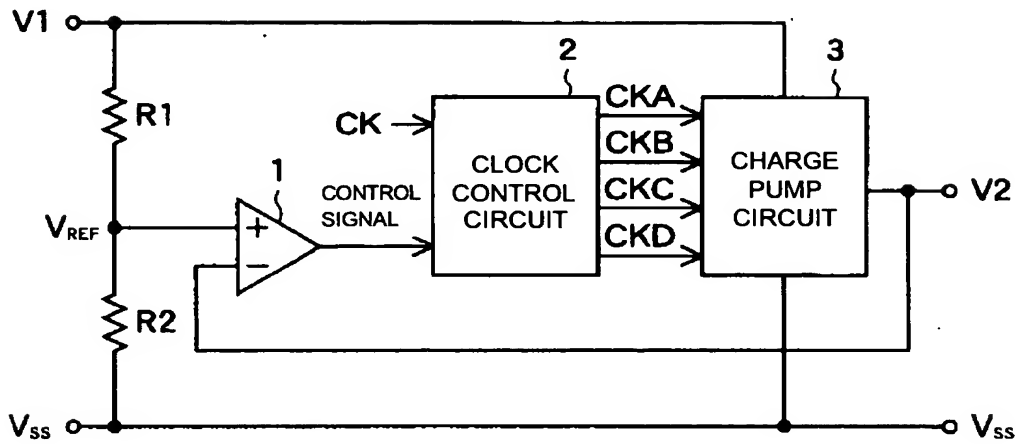
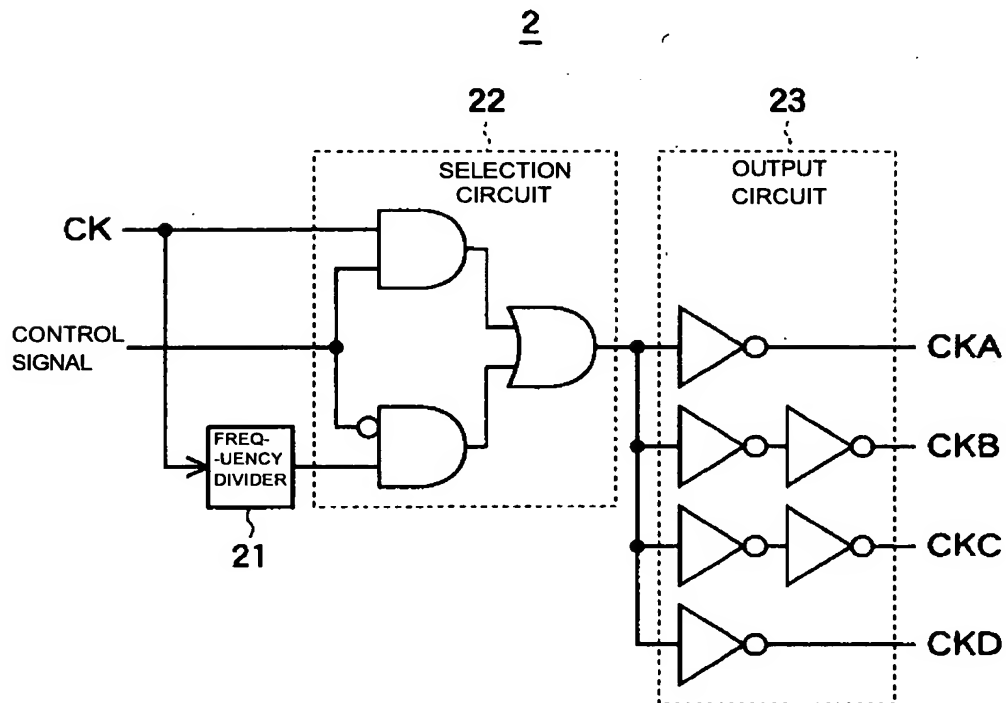


FIG. 2



The circuit diagram shows a multi-output voltage divider. A 'STABILIZED POWER SUPPLY CIRCUIT' (4) provides a regulated input voltage V_{REG} to the non-inverting input (+) of a first operational amplifier (5). The inverting input (-) of op-amp 5 is connected to a voltage divider consisting of resistors $R11$ and $R12$ connected to the output $V1$ and a common ground V_{SS} , respectively. The output of op-amp 5 is connected to a buffer (8) labeled 'X2', which provides a buffered output $V4$. A second voltage divider, consisting of resistors $R21$ and $R22$ connected to $V1$ and V_{SS} , provides an input to the non-inverting input (+) of a second operational amplifier (6). The inverting input (-) of op-amp 6 is connected to a voltage divider consisting of resistors $R31$ and $R32$ connected to $V4$ and V_{SS} , respectively. The output of op-amp 6 is connected to a buffer (9) labeled '1/2', which provides a buffered output $V6$. A third output $V3$ is taken from the node between $R21$ and $R22$. A fourth output $V5$ is taken from the node between $R31$ and $R32$. A fifth output $V2$ is taken from the common ground V_{SS} . A sixth output $V7$ is taken from the output of op-amp 6. A seventh output $V8$ is taken from the output of op-amp 5. A final output $V9$ is taken from the node between $R11$ and $R12$.

FIG.5

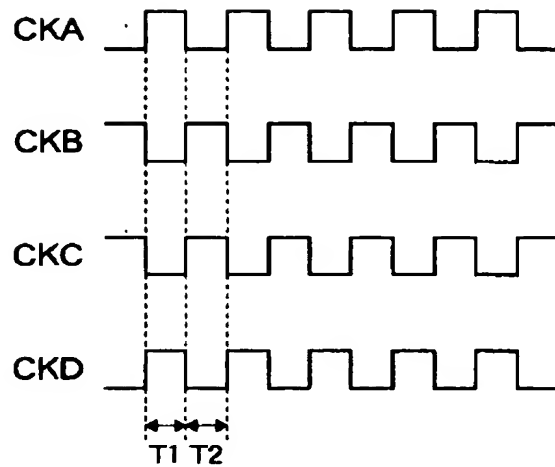


FIG.6 (a)

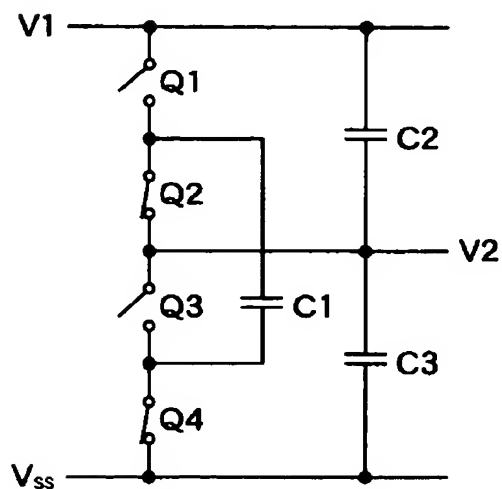


FIG.6 (b)

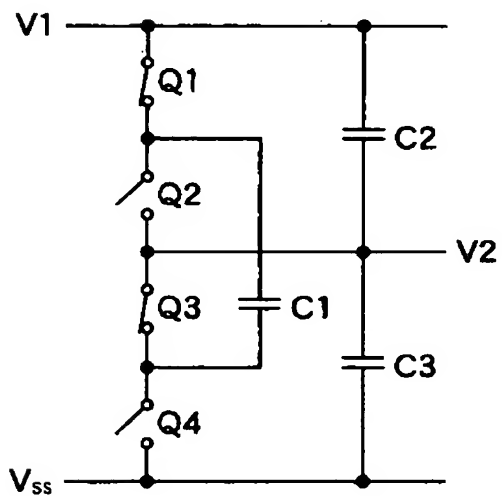


FIG.7

